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EXAMINER	
MAIS, MARK A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,324	LEE, JI YOUNG	
	Examiner	Art Unit	
	MARK A. MAIS	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-72* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-72* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 29, 2008 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 8-54, and 58-72 are rejected under 35 U.S.C. 102(e) as being anticipated by Baker et al. (USP 5,983,301).

4. With regard to claim 1, Baker et al. discloses a system for transferring a signal to a channel **[Fig. 1, signals from peripheral devices 14 to PCI bus 24 through ASIC 20 (Fig. 2)]**, comprising:

a storage unit **[Figs 2-3, General Receive FIFO 80 of FIFO 78]** associated with the channel **[Fig. 3, DMA Channels 0-3]** for storing source identification information **[Fig. 4, Word 0 (WD0) and Word 1 (WD1)]** of a plurality of sources **[Fig. 1, peripheral devices 14]** *the source identification information indicates* an order of priority of the plurality of sources for access to the channel **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**;

a plurality of selection circuits **[Fig. 4, combination of comparator logic 110 and priority encoder 128]** for receiving input signals from the sources, each of the selection circuits selecting one of the plurality of input signals **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**; and

a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel **[Fig. 3, 1394 receiver logic 102 receives channel output 130 from priority encoder 128, col. 13, lines 50-51]**.

5. With regard to claim 23, Baker et al. discloses a system for transferring a signals to channels **[Fig. 1, signals from peripheral devices 14 to PCI bus 24 through ASIC 20 (Fig. 2)]**, comprising;

a plurality of storage units **[Figs 2-3, General Receive FIFO 80 of FIFO 78]**, each storage unit being associated with one of the channels **[Fig. 3, DMA Channels 0-3]**, and each storage unit being adapted to store source identification information **[Fig. 4, Word 0 (WD0) and Word 1 (WD1)]** *indicating* an order of priority of the sources for access to the channel **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**;

for each of the plurality of channels, a plurality of selection circuits **[Fig. 4, combination of comparator logic 110 and priority encoder 128]** for receiving input signals from the sources **[Fig. 1, peripheral devices 14]**, each of the selection circuits selecting one of the plurality of input signals *in response to the source information* **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**; and

for each of the plurality of channels, a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel **[Fig. 3, 1394 receiver logic 102 receives channel output 130 from priority encoder 128, col. 13, lines 50-51]**.

6. With regard to claim 37, Baker et al. discloses a direct memory access (DMA) controller for controlling transfer of signals from input sources to output devices, a plurality of channels being connected to the output devices, the DMA controller **[Fig. 1, signals from peripheral devices 14 to PCI bus 24 through ASIC 20 (Fig. 2)]** comprising:

a plurality of storage units **[Figs 2-3, General Receive FIFO 80 of FIFO 78]**, each storage unit being associated with one of the channels **[Fig. 3, DMA Channels 0-3]**, and each storage unit being adapted to store source identification information **[Fig. 4, Word 0 (WD0) and Word 1 (WD1)]** *indicating* an order of priority of the sources for access to the channel **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**;

for each of the plurality of channels, a plurality of selection circuits **[Fig. 4, combination of comparator logic 110 and priority encoder 128]** for receiving input signals from the sources **[Fig. 1, peripheral devices 14]**, each of the selection circuits selecting one of the plurality of input *in response to source identification information* **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**; and

for each of the plurality of channels, a circuit for checking outputs of the selection circuits and forwarding selected input signals to the channel **[Fig. 3, 1394 receiver logic 102 receives channel output 130 from priority encoder 128, col. 13, lines 50-51]**.

7. With regard to claim 51, Baker et al. discloses a method for transferring a signal to a channel **[Fig. 1, signals from peripheral devices 14 to PCI bus 24 through ASIC 20 (Fig. 2); Fig. 3, DMA Channels 0-3]**, comprising:

storing **[Figs 2-3, General Receive FIFO 80 of FIFO 78]** source identification information **[Fig. 4, Word 0 (WD0) and Word 1 (WD1)]** for a plurality of sources **[Fig. 1, peripheral devices 14]** *the source identification information indicates* an order of priority of the plurality of sources for access to the channel **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**;

providing a plurality of selection circuits **[Fig. 4, combination of comparator logic 110 and priority encoder 128]** for receiving input signals from the sources **[Fig. 1, peripheral devices 14]**, each of the selection circuits selecting one of the plurality of input signals *in response to the source identification information* **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**;

with a checking circuit, checking outputs of the selection circuits and forwarding a selected input signal to the channel **[Fig. 3, 1394 receiver logic 102 receives channel output 130 from priority encoder 128, col. 13, lines 50-51]**.

8. With regard to claims 2 and 52, Baker et al. discloses that each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit **[Fig. 3, channel output 130 is valid after the OR logic circuit 129 generates a match on line 132]**.

9. With regard to claims 3 and 53, Baker et al. discloses that the storage unit is a register **[Fig. 2, FIFO 80 of FIFO 78]**.

10. With regard to claims 4 and 54, Baker et al. discloses that the storage unit stores the source identification information for the sources in order of priority of the sources for access to the channel **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**.

11. With regard to claims 8 and 58, Baker et al. discloses that the circuit checks the outputs of the selection circuits in a predetermined sequence **[Priority superisochronous logic continuously (predetermined sequence) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

12. With regard to claims 9 and 59, Baker et al. discloses that the circuit sequentially checks the outputs of the selection circuits **[Fig. 3, channel output 130 is valid after the OR logic circuit 129 generates a match on line 132]**.

13. With regard to claims 10 and 60, Baker et al. discloses that the sequence is determined by an order in which the source identification information of the sources is stored in the storage unit **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**.

14. With regard to claims 11 and 61, Baker et al. discloses that the circuit checks the outputs of the selection circuits in order of priority of the sources for forwarding input signals to the channel **[Fig. 3, 1394 receiver logic 102 receives channel output 130 from priority encoder 128, col. 13, lines 50-51; Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**.

15. With regard to claims 12 and 62, Baker et al. discloses that the system includes a plurality of channels **[Fig. 3, DMA Channels 0-3]**, input signals from the sources **[Fig. 1, peripheral devices 14]** being able to be forwarded to the plurality of channels.

16. With regard to claims 13 and 63, Baker et al. discloses a plurality of storage units **[Fig. 2, FIFO 80 of FIFO 78]** associated respectively with the plurality of channels **[Fig. 3, DMA Channels 0-3]**.

17. With regard to claims 14 and 64, Baker et al. discloses that each of the storage units **[Fig. 2, FIFO 80 of FIFO 78]** stores source identification information **[Fig. 4, Word 0 (WD0) and Word 1 (WD1)]** for sources that are able to forward input signals onto the channel associated with the storage unit **[Fig. 1, peripheral devices 14]**.

18. With regard to claims 15 and 65, Baker et al. discloses that the selection circuits are multiplexers **[multiplexes between multiple DMA channels, col. 14, lines 44-46]**.

19. With regard to claims 16 and 66, Baker et al. discloses that the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit **[Priority superisochronous logic continuously (predetermined sequence) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

20. With regard to claims 17 and 67, Baker et al. discloses that the multiplexers are ordered according to priorities of the sources for forwarding input signals to the channel **[Priority superisochronous logic continuously (predetermined sequence) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

21. With regard to claims 18 and 68, Baker et al. discloses that the sources are applied to inputs of the selection circuits according to a predetermined order **[Priority superisochronous logic**

continuously (predetermined sequence) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63].

22. With regard to claims 19 and 69, Baker et al. discloses that the predetermined order depends on priority of the sources for access to the channel **[Priority superisochronous logic continuously (predetermined sequence) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

23. With regard to claims 20 and 70, Baker et al. discloses that the source identification information **[Fig. 4, Word 0 (WD0) and Word 1 (WD1)]** is generated according to the predetermined order such that the selection circuits select the sources based on priority of the sources for access to the channel **[Priority superisochronous logic continuously (predetermined sequence) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

24. With regard to claims 21 and 71, Baker et al. discloses that a channel unit **[Fig. 3, FIFO 78]** associated with the channel for processing information related to the channel.

25. With regard to claims 22 and 72, Baker et al. discloses that the storage unit is part of the channel unit **[Fig. 3, FIFO 78]**.

26. With regard to claims 24 and 38, Baker et al. discloses that each selection circuit selects the selected input signal according to a state of a respective control input to the selection circuit **[Fig. 3, channel output 130 is valid after the OR logic circuit 129 generates a match on line 132]**.

27. With regard to claims 25 and 39, Baker et al. discloses that one or more of the sources **[Fig. 1, peripheral devices 14]** are allocated to one or more of the channels **[Fig. 3, DMA Channels 0-3]**.

28. With regard to claims 26 and 40, Baker et al. discloses that the allocation of the sources **[Fig. 1, peripheral devices 14]** to the channels **[Fig. 3, DMA Channels 0-3]** is controllable by controlling storage of source identification information in the storage units **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**.

29. With regard to claims 27 and 41, Baker et al. discloses that the storage units are registers **[Fig. 2, FIFO 80 of FIFO 78]**.

30. With regard to claims 28 and 42, Baker et al. discloses that each of the storage units stores its source identification information for the sources in order of priority of the sources for access to the associated channel **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**.

31. With regard to claims 29 and 43, Baker et al. discloses that the selection circuits are multiplexers **[multiplexes between multiple DMA channels, col. 14, lines 44-46]**.

32. With regard to claims 30 and 44, Baker et al. discloses that the multiplexers are ordered according to the sequence of the source identification information stored in the storage unit **[Priority superisochronous logic continuously (predetermined sequence) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

33. With regard to claims 31 and 45, Baker et al. discloses that the multiplexers are ordered according to priorities of the sources for forwarding input signals to the channels **[Priority superisochronous logic continuously (predetermined sequence) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

34. With regard to claims 32 and 46, Baker et al. discloses that the sources are applied to inputs of the selection circuits according to a predetermined order **[Priority superisochronous logic continuously (predetermined sequence) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

35. With regard to claims 33 and 47, Baker et al. discloses that the predetermined order depends on priority of the sources for access to the channels **[Priority superisochronous logic continuously (predetermined order) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

36. With regard to claims 34 and 48, Baker et al. discloses that the source identification information **[Fig. 4, Word 0 (WD0) and Word 1 (WD1)]** is generated according to the predetermined order such that the selection circuits select the sources based on priority of the sources for access to the channels **[Priority superisochronous logic continuously (predetermined order) examines the current context of all channels and assigns the channel with the highest priority having pending activity to the state machine for execution, col. 13, lines 59-63]**.

37. With regard to claims 35 and 49, Baker et al. discloses a plurality of channel units **[Fig. 3, FIFO 78]** associated respectively with the plurality of channels for processing information related to the channels.

38. With regard to claims 36 and 50, Baker et al. discloses that each of the storage units is part of one of the channel units **[Fig. 3, FIFO 78]**.

Claim Rejections - 35 USC § 103

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. Claims 5-7 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baker et al.

41. With regard to claims 5-7 and 55-57, Baker et al. does not specifically disclose that the registers **[Figs 2-3, General Receive FIFO 80 of FIFO 78]** store the source identifications **[Fig. 4, Word 0 (WD0) and Word 1 (WD1)]** in a scheme using most significant bits (MSBs) and/or least significant bits (LSBs). However, Applicants have not disclosed that using such a

MSB/LSB scheme solves any stated problem or is for any particular purpose other than an optimization of a known method of storing and/or searching for (priority) flags/indicators **[Fig. 4, header data contain WD0 and WD1 which are put through comparator logic 110 to select one of channels [0] through [N-1] and then through priority encoder 128 to output selected channel output 130, col. 13, line 64 to col. 14, line 41]**. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the storing and search scheme Baker et al. because such modifications are considered a mere design choice consideration, which fails to patentably distinguish over the prior art of Baker et al. In addition, the changing the scheme to use MSB/LSB for storing and searching for (priority) flags/indicators is interpreted as an optimum value for a known process. A discovery of an optimum value for a known process is obvious engineering. See In re Aller, 105 USPQ 233 (CCPA 1955).

Response to Arguments

42. Applicant's arguments with respect to claims 1-72 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

43. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

(a) Baker et al. (USP 6,006,286), System for controlling data packet transfers by associating plurality of data packet transfer control instructions in packet control list including plurality of related logical functions.

(b) Hayden et al. (USP 7,240,129), DMA controller having programmable channel priority.

44. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK A. MAIS whose telephone number is (571)272-3138. The examiner can normally be reached on M-Th 9am-8pm.

45. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing F. Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

46. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 4, 2009

/Mark A. Mais/
Examiner, Group Art Unit 2419

/Wing F. Chan/
Supervisory Patent Examiner, Art Unit 2419
2/5/09